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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/831,539	04/15/2002	Anand S. Murthy	42390.P6624PCT	6105

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07/30/2003

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EXAMINER

KEBEDE, BROOK

ART UNIT

PAPER NUMBER

2823

DATE MAILED: 07/30/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/831,539

Applicant(s)

MURTHY ET AL.

Examiner

Brook Kebede

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 May 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 11 and 13-30 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 11 and 13-30 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- ☐ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- ☐ Interview Summary (PTO-413) Paper No(s). _____
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: _____

DETAILED ACTION

Claim Objections

1. Claim 11 is objected to because of the following informalities:

Claim 11 recites the limitation “selectively forming a layer of a first material having the first conductivity type over the surface of recess” in lines 7-8. However, the limitation lacks proper antecedent basis. As suggestion, applicants advised the change “**the** first conductivity type” to --a first conductivity type-- in order to establish proper antecedent basis. Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 11 and 13-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 11 recites the limitation “selectively forming a layer of a first material having the first conductivity type over the surface of the recess, including the portion of the recess that underlies the gate electrode; and selectively forming a layer of a second material having a second conductivity type over the surface of the recess, including the portion that underlies the gate electrode” in lines 7-12.

It is not clear to the examiner how the second material can be formed over the surface of the recess since the first material is already formed over the surface of the recess. Is the claimed limitation calls for separate process steps for forming the first and second materials for different

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embodiments of or the first material first formed and the second material deposited over the first material. Therefore, the recited claimed limitation lacks clarity in its meaning and scope and the claim is indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 13-21 are also rejected as being dependent of the rejected independent base claim.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 22-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Horiuchi et al. (JP/63076481).

The rejection that was set forth in Paper No. 12 is maintained and repeated herein below as record.

Re claim 22, Horiuchi et al. disclose a method of making a transistor, comprising: forming a dielectric (3) on a first surface of a wafer (1); forming a conductive layer (4) overlying the dielectric (3); patterning the conductive layer (4) and dielectric (3) so as to form a gate structure (see Fig. 3B); forming recesses (not labeled) adjacent and partially subjacent the gate structure (3 4 5 18); and in a continuous operation, back filling the recesses with doped crystalline material (9 10 91 101); wherein back filling comprises forming crystalline material of at least a first conductivity type (see Figs. 3B-3D).

Re claim 23, as applied to claim 22 above, Horiuchi et al. disclose all the claimed limitations including the limitation wherein the crystalline material of the first conductivity type

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is selected from the group consisting of p-type silicon, p-type silicon germanium, n-type silicon, and n-type silicon germanium (see Figs. 3B-3D).

Re claim 24, as applied to claim 22 above, Horiuchi et al. disclose all the claimed limitations including the limitation wherein back filling further comprises forming crystalline material of a second conductivity type (see Figs. 3B-3D).

Re claim 25, as applied to claim 22 above, Horiuchi et al. disclose all the claimed limitations including the limitation wherein the crystalline material of the second conductivity type is selected from the group consisting of p-type silicon, p-type silicon germanium, n-type silicon, and n-type silicon germanium (see Figs. 3B-3D).

Re claim 26, as applied to claim 25 above, Horiuchi et al. disclose all the claimed limitations including the limitation wherein back filling comprises a selective deposition (see Figs. 3B-3D).

Re claim 27, Horiuchi et al. disclose a method of fabricating a FET, comprising: forming a gate electrode having side walls over a gate insulator on a surface of a semiconductor substrate having a first conductivity type; forming first spacers along the sidewalls of the gate electrode; forming a recess that extends vertically down into the substrate and extends laterally through the substrate so as to underlie a portion of the gate electrode, the recess having a substrate surface; substantially filling the recess with a first layer of doped crystalline material, the first layer having a second conductivity type (see Figs. 3B-3D).

Re claim 28, as applied to claim 27 above, Horiuchi et al. disclose all the claimed limitations including the limitation further comprising depositing the first layer of doped crystalline material until a vertical distance between a top surface of the first layer and the

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surface of the substrate is greater than a vertical distance between a top surface of the gate insulator and the surface of the substrate (see Figs. 3B-3D).

Re claim 29, as applied to claim 27 above, Horiuchi et al. disclose all the claimed limitations including the limitation forming a second layer of doped crystalline material over the substrate surface of the recess, the second layer having the same conductivity type as the semiconductor substrate, and the second layer having a doping concentration that is greater than a doping concentration of the semiconductor substrate near the substrate surface of the recess (see Figs. 3B-3D).

Re claim 30, as applied to claim 29 above, Horiuchi et al. disclose all the claimed limitations including the limitation wherein forming a recess comprises placing the substrate in a parallel plate reaction chamber with a gap of approximately 1.1 cm, an RF power in the range of approximately 50 W to 200 W, a pressure greater than approximately 500 mT, and plasma etching with sulfur hexafluoride and helium (see Figs. 3B-3D).

Allowable Subject Matter

6. Claim 11 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action.

7. Claims 13-21 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Response to Arguments

8. Applicant's arguments with respect to claims 11 and 13-21 have been considered but are moot in view of the new ground(s) of rejection that was necessitated by the amendment filed on May 12, 2003 in Paper No. 13.

With respect to claim 22, applicants argued that “Horiuchi does not teach ...back filling the recesses, including the portion of the recesses that partially subjacent the gate structure, with doped crystalline material.”

In response to the applicants’ argument, the Examiner respectfully submits that such an argument is not commensurate with the scope of the claims, in particularly, as stated above. The Examiner respectfully submits that Horiuchi et al. disclose all the claimed limitation as applied herein above. As shown Fig. 3D both layers 9 91 and 10 101 uses as source/drain electrode are arsenic (As) doped amorphous silicon layer which crystallized during annealing and also Fig. 3D clearly teaches the limitation of “back filling the recesses, including the portion of the recesses that partially subjacent the gate structure, with doped crystalline material” is clearly in addition see the specification in Pages 407-408.

Furthermore, applicants’ argument with respect to claim 27 has no merit because Horiuchi et al. also disclose the limitation “substantially filling the recess that extends laterally through the substrate so as to underlie a portion of the gate electrode with a first layer doped crystalline material (see Fig. 3D).

Therefore, the rejection under 35 U.S.C. 102 is deemed proper.

Conclusion

9. Applicants’ amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

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the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Correspondence

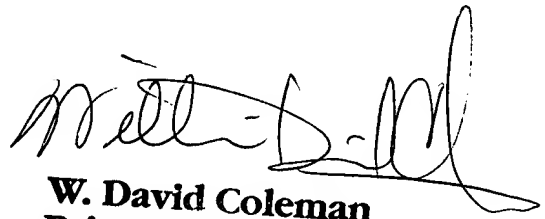
10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (703) 306-4511. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703) 306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Brook Kebede

BK
July 25, 2003


W. David Coleman
Primary Examiner